We claim:

1. A semiconductor structure comprising:
a substrate; and,
a plurality of conductive elements buried within the substrate.

2. The structure of claim 1, wherein at least one of the conductive elements is metal.

3. The structure of claim 2, wherein the metal comprises one of tungsten and a tungsten alloy.

4. The structure of claim 2, wherein the metal comprises one of a non-radioactive element selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and an alloy of the non-radioactive element.

5. The structure of claim 1, wherein each of the plurality of conductive elements is oriented in one of an x plane and a y plane.

6. The structure of claim 1, wherein the substrate comprises doped silicon.

7. The structure of claim 1, further comprising silicon-on-insulator elements above at least one of the conductive elements.

8. The structure of claim 1, further comprising insulating material surrounding the conductive elements.

9. The structure of claim 8, wherein the insulating material is selected from the group consisting of: oxide, oxy-nitride, and nitride.

10. The structure of claim 1, wherein at least two of the plurality of conductive elements are connected to one another.

11. A semiconductor device comprising:

a substrate; and,

a plurality of conductive layers buried within the substrate.

12. The semiconductor device of claim 11, wherein each conductive layer comprises at least one conductive element.

13. The semiconductor device of claim 11, wherein the plurality of conductive layers comprises:

a first layer having lines oriented in a first direction; and,

a second layer positioned above the first layer and having lines oriented in a second direction orthogonal to the first direction.

14. The semiconductor device of claim 13, wherein the plurality of conductive layers further comprises a third layer positioned above the second layer and having lines oriented in a third direction orthogonal to one of the first direction and the second direction.

15. The semiconductor device of claim 11, further comprising a silicon-on-insulator layer above at least one of the conductive layers.

16. The semiconductor device of claim 11, wherein the semiconductor device comprises a memory device.

17. The semiconductor device of claim 16, wherein the memory device is selected from the group consisting of: dynamic random-access memory (DRAM),

static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM).

18. A method comprising:

a) forming at least one first trench within a semiconductor substrate at a first depth;

b) depositing a first conductive material substantially at the bottom of each first trench;

c) forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth; and,

d) depositing a second conductive material substantially at the bottom of each second trench.

19. The method of claim 18, wherein the first conductive material is identical to the second conductive material.

20. The method of claim 18, wherein at least one of the first conductive material and the second conductive material comprises one of tungsten and a tungsten alloy.

21. The method of claim 18, further comprising between a) and b), depositing a seed material to facilitate deposition of the first conductive material.

22. The method of claim 21, wherein the seed material comprises titanium.

23. The method of claim 21, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

24. The method of claim 18, further comprising between c) and d), depositing a seed material to facilitate deposition of the second conductive material.

25. The method of claim 24, wherein the seed material comprises titanium.

26. The method of claim 24, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

27. The method of claim 18, further comprising between b) and c), depositing an insulative material within each first trench over the first conductive material.

28. The method of claim 27, wherein the insulative material comprises silicon dioxide.

29. The method of claim 18, further comprising after d), depositing an insulative material within each second trench over the second conductive material.

30. The method of claim 29, wherein the insulative material comprises silicon dioxide.

31. The method of claim 18, further comprising between a) and b), forming an insulating layer at the bottom of and on walls of each first trench.

32. The method of claim 31, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each first trench.

33. The method of claim 18, further comprising between c) and d), forming an insulating layer at the bottom of and on walls of each second trench.

34. The method of claim 33, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each first trench.

35. The method of claim 18, wherein at least one of the first conductive material and the second conductive material is deposited by a selective deposition process.

36. The method of claim 35, wherein the selective deposition process is selected from the group essentially consisting of chemical vapor deposition and plating.

37. The method of claim 18, wherein the semiconductor substrate is part of a wafer having a front side and a back side, and further comprising after d), thinning the back side of the wafer to expose at least one of the first conductive material and the second conductive material.

38. The method of claim 18, further comprising after d), connecting at least one of the first conductive material with at least one of the second conductive material.

39. A method comprising:

burying first conductive elements within a semiconductor substrate at a first depth; and,

burying second conductive elements within a semiconductor substrate at a second depth less than the first depth.

40. The method of claim 39, wherein the first conductive elements and the second conductive elements each comprise a predetermined material.

41. The method of claim 39, wherein each of burying first conductive elements and burying second conductive elements comprises:

forming at least one trench within a semiconductor substrate, each trench having walls and a bottom;

forming an insulating layer at the bottom and on the walls of the trench;

depositing a seed material at the bottom of each trench;

depositing a conductive material within each trench over the seed material; and,

depositing an insulative material within each trench over the conductive material.